CLAIMS

What is claimed is:

- 1 A common mode feedback circuit apparatus comprising:
- a first and a second node defining a differential node pair; and 2
- a collective plurality of transconductors including a first plurality of 3
- transconductors associated with the first node and a second plurality of 4
- transconductors associated with the second node, wherein at least one 5
- transconductor of the collective plurality has an adjustable transconductance, 6
- wherein the total transconductance of each of the first and second pluralities 7
- is nominally halved between any adjustable transconductors and the 8
- remaining transconductors of that plurality. 9
- The apparatus of claim 1 wherein the total transconductance of each of 1 2.
- 2 the first and second pluralities is nominally halved between the set of
- transconductors capable of being decoupled from its associated node and 3
- recoupled to a complementary node and the remaining transconductors of 4
- 5 that plurality.

repeatel lain (1) = 5 The apparatus of claim 1 wherein each of the first and second plurality 1 3.

of transconductors includes at least one transconductor with an adjustable 2

3 transconductance.

1	4.	The apparatus of	claim/3 further	comprising:
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- a calibration engine, wherein while in a calibration mode the
- 3 calibration engine varies each of the adjustable transconductances until a
- 4 sensed differential voltage across the differential node pair is substantially
- 5 zero.
- 1 5. The apparatus of claim 4 further comprising:
- 2 a calibration signal/source; and
- a plurality of switches for switching between a calibration mode and a
- 4 normal mode, wherein while in calibration mode the switches couple a
- 5 common mode voltage signal from a common mode node to non-adjustable
- 6 transconductors of the first and second pluralities, wherein the switches
- 7 couple each of the adjustable transconductors to their complementary nodes,
- 8 wherein the switches couple the calibration signal voltage source to the
- 9 adjustable transconductors, wherein a current generated by the adjustable
- 10 transconductors is proportional to the calibration signal voltage source,
- 11 wherein the calibration signal voltage source is independent of the common
- 12 mode voltage signal.
- 1 6. The apparatus of claim 5 wherein while in normal mode the plurality
- 2 of switches decouple the adjustable transconductors from the calibration
- 3 signal voltage source, decouple the adjustable transconductors from their
- 4 complementary nodes, and couple the adjustable transconductors to their
- 5 respective associated differential nodes.

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- 1 7. The apparatus of claim 1 wherein each of the first plurality and second
- 2 plurality comprises 2 transconductors.
- 1 8. The apparatus of claim 7 wherein every transconductor of the
- 2 collective plurality has substantially a same nominal transconductance value.
- 1 9. The apparatus of claim 1 wherein the circuitry is implemented on an
- 2 integrated circuit semiconductor die.
- 1 10. The apparatus of claim 9 wherein the integrated circuit is a
- 2 complementary metal oxide semiconductor (CMOS) integrated circuit.
- 1 11. The apparatus of claim 1 further comprising:
- a calibration engine, wherein the calibration engine varies the
- 3 adjustable transconductance of the at least one transconductor until a sensed
- 4 differential voltage across the differential node pair is substantially zero.
- 1 12. The apparatus of claim 11 wherein the calibration engine further
- 2 comprises a band pass filter to sense the differential voltage at a pre-
- 3 determined frequency.

- 1 13. A method of calibrating a common mode feedback block circuit,
- 2 comprising the steps of:
- a) providing a common mode feedback block apparatus having a
- 4 first node and a second node forming a differential node pair, the apparatus
- 5 further comprising a collective plurality of transconductors including a first
- 6 plurality of transconductors associated with the first node and a second
- 7 plurality of transconductors associated with the second node, the collective
- 8 plurality including at least one adjustable transconductor; and
- 9 b) adjusting the at least one adjustable transconductor until a
- 10 differential voltage across the differential node pair is substantially zero.
 - 1 14. The method of claim 13 wherein step b) is performed while the
 - 2 common mode feedback block is in a calibration mode.
- 1 15. The method of claim 13 wherein step b) further comprises the step of
- 2 sensing the differential voltage only at a pre-determined frequency.
- 1 16. The method of claim 13 further comprising the step of:
- 2 c) switching the common mode feedback block to a normal mode
- 3 to prevent further transconductance adjustments to the at least one adjustable
- 4 transconductor.
- 1 17. The method of claim 13 wherein each of the first and second nodes has
- 2 at least one associated adjustable transconductor, wherein step b) further

- includes the step of adjusting each of the associated adjustable 3
- transconductors until the differential voltage across the differential node pair 4
- is substantially zero. 5
- The method of claim 14 wherein the adjustable transconductors are 1 18.
- 2 adjusted by increasing a transconductance of a transconductor associated with
- the first node by an amount δ and decreasing a transconductance of a 3
- 4 transconductor associated with the second node by the amount δ .

need to be defined

- 19. 1 The method of claim 13 further comprising the step of:
- 2 providing a calibration signal source independent of a common
- mode node, wherein during calibration the calibration signal source provides 3
- 4 a control voltage for the adjustable transconductors, wherein the common
- mode node provides the control voltage for the remaining transconductors of 5
- the collective plurality of transconductors. 6
- 1 20. The method of claim 19 wherein the calibration signal source and the
- 2 common mode feedback block reside on a same integrated circuit die.